# MAINTENANCE MANUAL
# FOR
# I/O BOARD
# 19D902573G1

## TABLE OF CONTENTS


| | Page |
|---|---|
| SPECIFICATIONS | Front Page & 1 |
| DESCRIPTION | 1 |
| Jumper Configuration And Setup | 1 |
| Radio Control And Interface | 1 |
| Siren/Light Serial & Parallel Outputs | 1 |
| 5-Volt Regulators And Reset | 2 |
| Power Relay | 2 |
| Power Distribution | 2 |
| RF Bypass Capacitors | 2 |
| I/O Signal Line Protection | 3 |
| TROUBLESHOOTING | 3 |
| Tone Deviation Adjustment | 3 |
| IC DATA | 4 |
| OUTLINE DIAGRAM | 5 |
| PARTS LIST | 6 |
| SCHEMATIC DIAGRAM | 7 |


## SPECIFICATIONS*

| | |
|---|---|
| Input Power | |
| A+ (J1-11) | 13.8 VDC ±20% |
| A+ IGN (J1-16) | 13.8 VDC ±20% |
| Output Power | |
| SW A+ | 13.8 VDC ±20% |
| +5V | 5.0 VDC ±5% |
| TX-SW-IGN | 13.6 VDC ±20% |
| Maximum Input Current Drain | |
| A+ | |
| With Radio | 3.0 amperes |
| Without Radio | 350 milliamperes |
| A+ IGN | 20 milliamperes |

Continued

Ericsson GE Mobile Communications Inc.
Mountain View Road • Lynchburg, Virginia 24502

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## SPECIFICATIONS*
**(Continued)**

| | |
|---|---|
| Maximum Output Current Drain | |
| SW A+ | 2.65 amperes |
| +5 VOLTS | 350 milliamperes |
| Temperature Range | -30°C TO +60°C<br>(-22°F TO +140°F) |
| Logic Levels | |
| High (1) | 4.0 Volts ±1.0 volt |
| Low (0) | 0.5 Volts ±1.0 Volt |
| Reset Pulse Duration | 30 milliseconds ±10 MS |
| Light Relay Drivers | |
| Current Sink (Maximum) | 200 Milliamperes |
| Low Voltage (Maximum) | 1.5 Volts |
| Audio Input/Output | 100 Millivolts at 5%<br>distortion maximum |
| Encode Tone Audio | 0-3 Volts RMS, at 5%<br>distortion maximum |
| Public Address Audio | |
| SPKR1/SPKR2 Input | 6.2 Volts RMS |
| PA Audio High | 2.0 Volts RMS ±1.0 Volt |
| Distortion | 5% maximum |

* These specifications are intended primarily for use by service personnel. Refer to the appropriate Specification Sheet for complete specifications.

## DESCRIPTION

I/O (Input/Output) Board 19D902573G1 provides the interface between the microcomputer board and all external equipment used with the S-825 EDACS System or Scan control unit. The I/O board interfaces the following equipment, if present:

- RANGR EDACS mobile radio
- Vehicular Repeater
- Mobile Siren/Light/PA unit
- Dual control unit
- Voice Guard unit
- Mobile Data unit
- Handset/Hookswitch
- Internal/External speaker
- External status/message inputs
- PC (Personal Computer) programmer

The control unit is connected to the radio and other external equipment through jacks on the I/O board. J1 on the I/O board connects the control unit to power, internal speaker, external speaker, and other optional equipment. J2 connects the control unit to the radio. J3 connects the control unit to Voice Guard, mobile data terminal, dual control, vehicular repeater and other options. J5 connects the control unit to an optional Siren/Light unit, and to the PC Programmer.

The processor board writes to registers on the I/O board to perform the interface functions to the radio system. The microprocessor is connected to J6 on the I/O board through a 26-pin ribbon cable.

The first register provides the mobile siren/light controls. Parallel Darlington drivers (U11 and U12) are used to interface the siren/light relay controls. This register also controls the power relay.

The second register controls the serial data to the radio, and is the heart of the EDACS system. The three-wire, 9600 baud serial bus provides the communication path between the S-825 EDACS control unit and the RANGR mobile radio.

The last register generates the encode tones. The tone output level is set by Tone Deviation Adjust R23.

Sampling of the input lines is performed through an analog multiplexer. Up to eight separate radio system inputs are multiplexed onto a single line to the processor board.

An audio amplifier provides the audio drive to the siren/PA.

A relay controls the power to the control unit by switching the continuous A+ power to the A+ switched power. This also provides power to the logic devices on the I/O board and the rest of the Control Unit through a 5-Volt regulator.

## JUMPER CONFIGURATION AND SETUP

Jumpers on the I/O board configure the control unit for the various options used. Table 1 shows the jumper configuration for the various options.

Table 1 - Jumper Configuration

| JUMPER | POSITION OF PLUG | FUNCTION OR OPTION |
|---|---|---|
| J7 | 1 & 2<br>2 & 3 | Group Down<br>Default (Spkr 2) |
| J8 | 1 & 2<br>2 & 3 | Default<br>Handset/Hookswitch |
| J9 | 1 & 2<br>2 & 3 | Default<br>Handset/Hookswitch |
| J10 | 1 & 2<br><br>2 & 3 | Dual Contr. w/Parallel Audio<br>Default (INDV AUDIO) |

## RADIO CONTROL AND INTERFACE

The I/O board provides the control and interface to the mobile radio. The mobile radio system control functions are derived from registers U3, U4, and U5. The mobile radio system outputs are sampled through the analog multiplexer U1. The mobile radio audio interface is accomplished through the received radio audio and the microphone audio. In addition, several input/output signals from the processor board are applied with the I/O board serving as a buffer.

The microphone, although not part of the mobile radio, provides inputs to the control unit to perform the radio control and interface.

## SIREN/LIGHT SERIAL & PARALLEL OUTPUTS

The control unit provides two types of outputs for siren and light controls; both serial and parallel outputs. The serial output provides for full control of an optional Siren/Light unit.

CAUTION

An EMF protection diode must be installed with each relay that is driven by a Darlington driver.

The parallel control consists of five parallel outputs (U3, U11, U12). These are Darlington outputs that may be used to turn on relays for control of individual lights, trunk release, sirens, etc.

## TX TONE GENERATION

A five-bit Digital/Analog generator (U5) is used to generate DTMF and GESTAR encode tones. The generated tones are adjusted to the desired deviation level by R23.

The transmit audio may be switched from either the microphone audio or the five bit D/A register.

## RADIO SERIAL BUS

A three wire, 9600-baud serial bus is the heart of the S-825EDACS/ radio system. This bus provides the communication path between the control head (slave), and the radio (master). When the control unit wishes to talk to the mobile, the service request line is activated. The mobile then polls the control unit for the information.

## STATUS/MESSAGE SERIAL BUS

This four-wire serial bus (R39, Q4, Q5 and Q6) is used to communicate to any external switches.

## SIREN/LIGHT PA AUDIO

The PA audio is derived from the two speaker signals. This audio may be the external 10-watt radio speaker, or the optional Siren/Light PA may be used to provide an output of 50 watts.

## 5-VOLT REGULATORS AND RESET

The digital 5-Volt regulator/reset circuit on the I/O board consists of U7, C10, and C9.

U7 is a +5-Volt regulator with an external reset output. The reset output is an open collector active low signal that is used to initialize the registers on the I/O board as well as the processor board at a power up and power down condition. Capacitor C10 provides the delay time for the reset pulse generated by U7.

On a power down condition, the reset output pulse from U7 is generated when the output voltage (5 volts nominal) drops to about 4.75 volts.

At a power up condition, the reset output is held low until the output voltage reaches a nominal 5 volts. At that point, the reset output is held low until a specified delay time has expired.

The regulator reset pulse RESET is or-tied with the watchdog timer reset pulse generated from the processor board.

The second 5-volt regulator is the audio voltage supply.

## RELAYS

There are two relays (K1 and K2) on the I/O board. Relay K1 is the power relay. Relay K2 controls the switched A+ for the radio system. The relay is activated by the PWR switch on the front of the control unit. The microprocessor RELAY-CTRL output control turns the relay on and off.

### Power Relay

Relay K1 is used to switch the continuous A+ battery power to the switched power supply SW A+. The switched power (SW A+) supplies input power to devices on all three boards of the control unit either directly or through the +5 volt regulator, U1.

When the control unit is powered down, the A+ power supply drain in the control unit is on the processor board through its relay control flip flop. The processor board relay control flip flop generates RELAY-CTRL which is a low (approximately 0 volts) or a high (approximately 10 volts) level.

RELAY-CTRL is one input to Darlington driver U11. The output of at U11-16 is applied to the relay coil, K2-16.

When RELAY-CTRL is high, RLY is low and pulls current through the relay coil. The relay contacts close and routes A+ power to the SW A+ line. When RELAY-CTRL is low, RLY is high and floats the relay coil high to A+. The relay contacts open and disconnects the A+ continuous power from the SW A+.

### Audio/Speaker Relay

The routing of audio to the internal or external speaker is performed by relay K1. The control line for the internal or external speaker is SPKR CONTROL.

When the control line is low, the SPKR1 FROM RADIO line is routed to the SPKR1 TO HKSW LINE, and to SPKR1 TO VEHICLE (through jumper J8). When the control line is high, the SPKR1 FROM RADIO line is routed to the EXT SPKR1 line.

## POWER DISTRIBUTION

The power supply used by the I/O board of the control unit includes A+. The power supply, IGN-A+, is sensed by the control unit to enable/disable the transmit power and siren functions.

The power supplies generated by the I/O board include SW A+ and +5V.

The A+ power is the continuous battery power. This A+ power is input to the relay control flip-flop on the microprocessor board, and energizes the coil of relay K2 through the Darlington driver.

SW A+ power is the switched A+ power which enables the control unit to be turned on and off. The SW A+ power is generated from the A+ power through the relay K2. The SW A+ is used to generate the +5-volt power through regulator U7, power the LED's on the keypad board, and power the EL driver on the processor board.

The +5-Volts is generated from the SW A+ power through 5-volt regulator U7. This power supply is the 5-volt logic power for devices on the I/O board, the processor board, and the keypad board of the control unit, and provides a stable reference voltage for the LCD temperature compensation circuit and the photodetector circuit on the keypad board.

The grounds used on the I/O board are GND (logic ground) and MIC -LO (microphone audio ground). Figure 1 shows the system interface for the I/O board.

## RF BYPASS CAPACITORS

The I/O board is interfaced to the processor board of the control unit, to the mobile radio, to the power system of the vehicle or motorcycle, to the vehicular repeater system, to the microphone, and to the siren/PA unit. Therefore, RF bypass capacitors are provided to filter the fast switching digital signals and to prevent radio frequency noise bursts from corrupting the digital signals.

The sensitive signals that are bypassed include those on the connectors that the I/O board interfaces with.

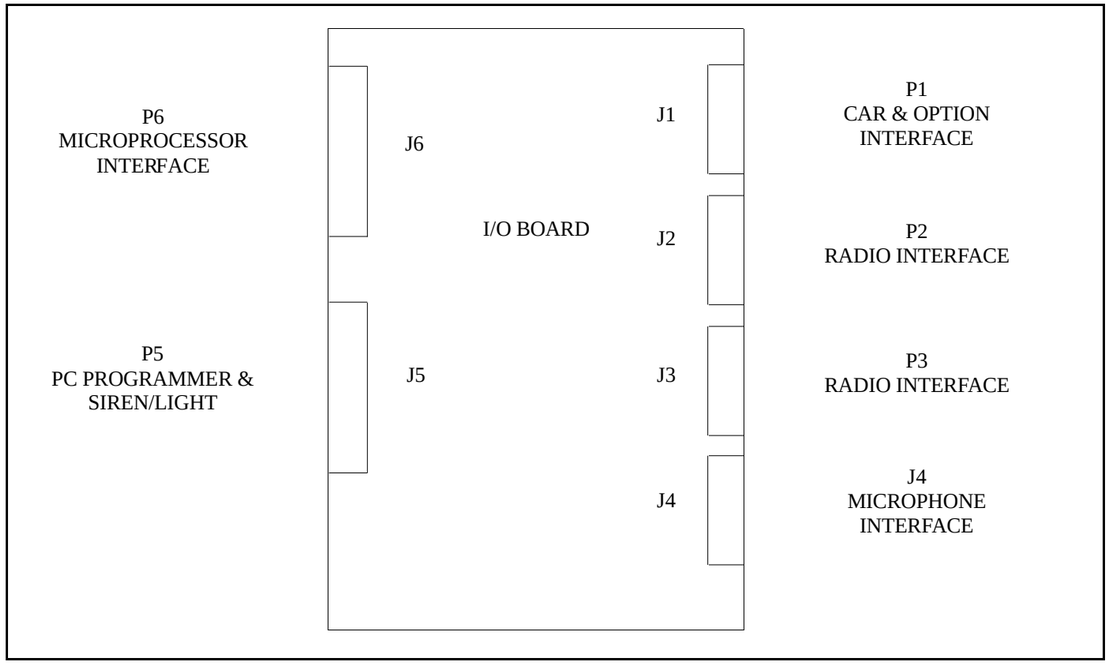



Figure 1 - I/O Board/System Interface

## I/O SIGNAL LINE PROTECTION

The I/O board employs diode protection on input and output lines in order to prevent excessive noise voltage spikes from causing damage to the control unit components from the environment.

The sensitive signals that are diode protected are those on the J1, J2, J3, J4, and J5 connectors interface the I/O board with the radio system units outside of the control unit.

# DIGITAL INPUTS

The I/O board receives digital inputs through an 8-bit mux, U1. The input signals are:

1) MICROPHONE PTT
2) CHANNEL GUARD DISABLE
3) GROUP DOWN
4) CONTROL UNIT TEST MODE
5) MOBILE TEST MODE
6) EMERGENCY FLOOR SWITCH
7) IGNITION A+
8) GROUP UP

## DIGITAL I/O DESCRIPTIONS

The data bus, consisting of J6-1 through J6-10 acts as a parallel port when writing to U5, and as a serial port when writing to registers U3 or U4. U1 is an audio mux that is used to input digital signals one at a time. A block diagram of the digital input/output devices is shown in Figure 2.

## READING FROM INPUT MUX U1

Reading from audio mux module U1 is accomplished by providing an address on J6 pins 1, 2, and 3 and then activating J6 pin 4 as the inhibit line. The input data from each of the 8 inputs is read from AUDIO MUX (J6-16).

## SERIAL OUTPUT REGISTERS U3 AND U4

Writing to 8-bit latches U3 and U4 is accomplished by providing an address on J6 pins 1, 2, and 3 and then activating J6 pin 7 for U3 and J6 pin 8 for U4. The data to be output at each address is presented on J6 pin 4 for both ICs. RESET (J6-26) must be verified high in order to write any data.

## PARALLEL OUTPUT REGISTER U5

Writing to parallel output register U5 is accomplished by providing data on J6 pins 1, 2, 3, 4, 5, and 6, and then activating J6 pin 8 to latch the data (device is edge triggered). RESET (J6-26) must be verified high in order to write any data. If RESET is a "0", then the outputs are all "0".

Five of the six outputs form a five bit D/A. They are used for transmit tone generation. This is accomplished by weighting each bit by a different summing resistor and then performing a level adjustment by potentiometer R23. The output of R23 is then buffered by op amp U10A, and then switched onto the MIC HI COMBINED (J2-5) line via transistor switch Q8. Q8 is controlled by Q10 and TONE SELECT (U5-15 = "1").

If the TONE SELECT line is set equal to "0", then the MIC HI (J4-4) is switched onto the MIC HI COMBINED (J2-5) via transistor switch Q9. Q9 is controlled by Q12.

# TROUBLESHOOTING

A functional test procedure for the I/O board consists of exercising the board using a "dumb" terminal and the MONITOR test software. The MONITOR software is part of the operational code. Instructions for the MONITOR tests and power continuity checks are contained in Combination Manual LBI-38445.

## TONE DEVIATION ADJUSTMENT

1. Remove the weatherproof screw and washer located below microphone connector J4 on the back of the control unit.
2. Turn the control unit On. Next, select a conventional system using the SYS push-button. Then select a conventional channel using the GROUP push-button.
3. Set up a receiver monitor on the transmit frequency. Then initiate the GESTAR or DTMF signaling and measure the tone deviation on the monitor.
4. If required, adjust R23 to set the tone deviation level between 1 kHz and 3 kHz (or to the proper level for your system).
5. Replace the weatherproofing screw and washer.

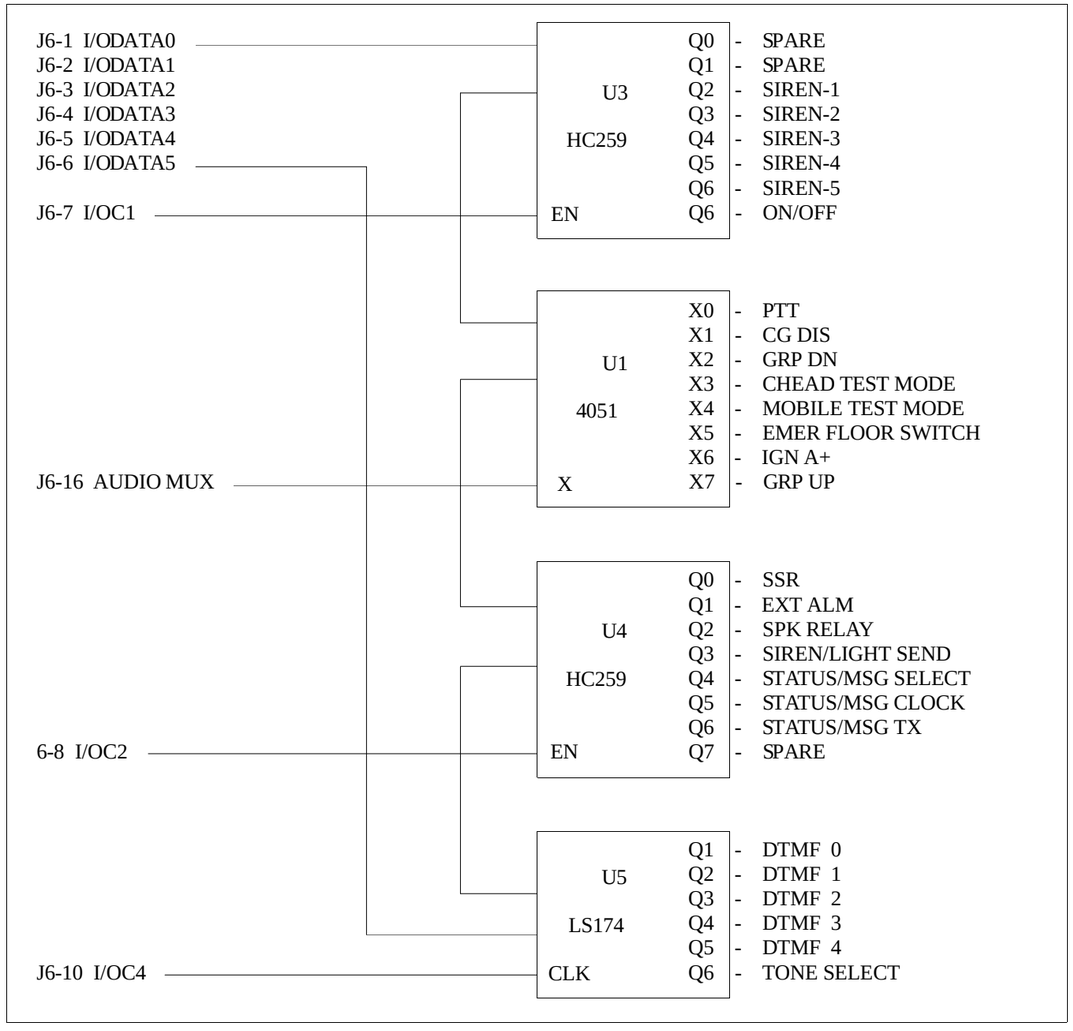
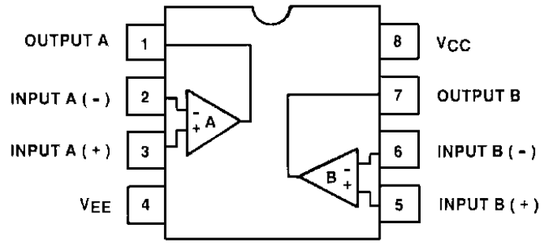
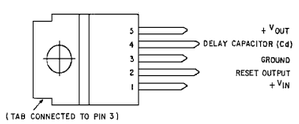


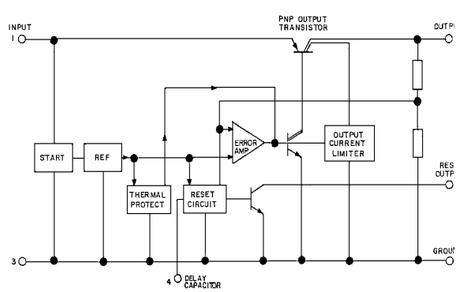

Figure 2 - I/O Board System Logic Layout

### OPERATIONAL AMPLIFIER U10
### 19A701789P2

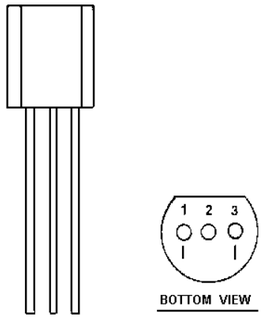



### VOLTAGE REGULATOR U7
### 19A704970P1




### VOLTAGE REGULATOR U9
### 19A704971P1




PIN IDENTIFICATION

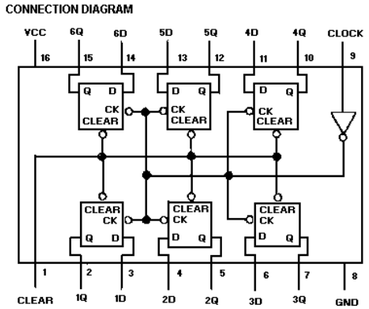
PIN 1. OUTPUT
PIN 2. GROUND
PIN 3. INPUT

### HEX DATA FLIP-FLOP U5
### 19A704380P9

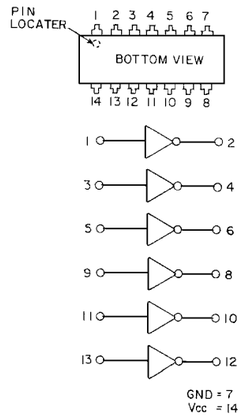
TRUTH TABLE

| INPUTS | | | OUTPUTS |
|---|---|---|---|
| CLEAR | CLOCK | D | Q |
| L | X | X | L |
| H | I | H | H |
| H | I | L | L |
| H | L | X | Q |

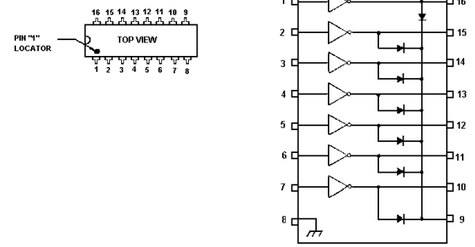
CONNECTION DIAGRAM



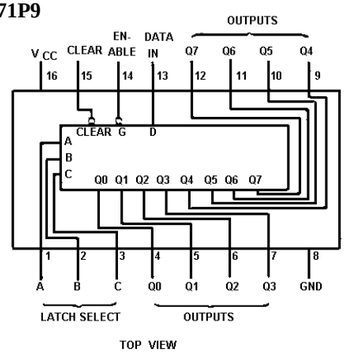

### HEX INVERTER U6
### 19A116180P75




### DARLINGTON INTERFACE U11, U12
### 19A134693P1




### LATCH/DECODER U3, U4
### 19A703471P9

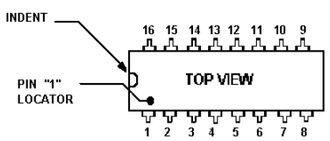


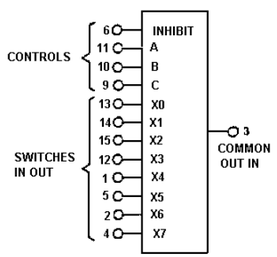

TOP VIEW

TRUTH TABLE

| Inputs | | Outputs of Addressed Latch | Each Other Output | Function |
|---|---|---|---|---|
| Clear | $\overline{G}$ | | | |
| H | L | D | $Q_{i0}$ | Addressable Latch |
| H | H | $Q_{i0}$ | $Q_{i0}$ | Memory |
| L | L | D | L | 8-Line Decoder |
| L | H | L | L | Clear |

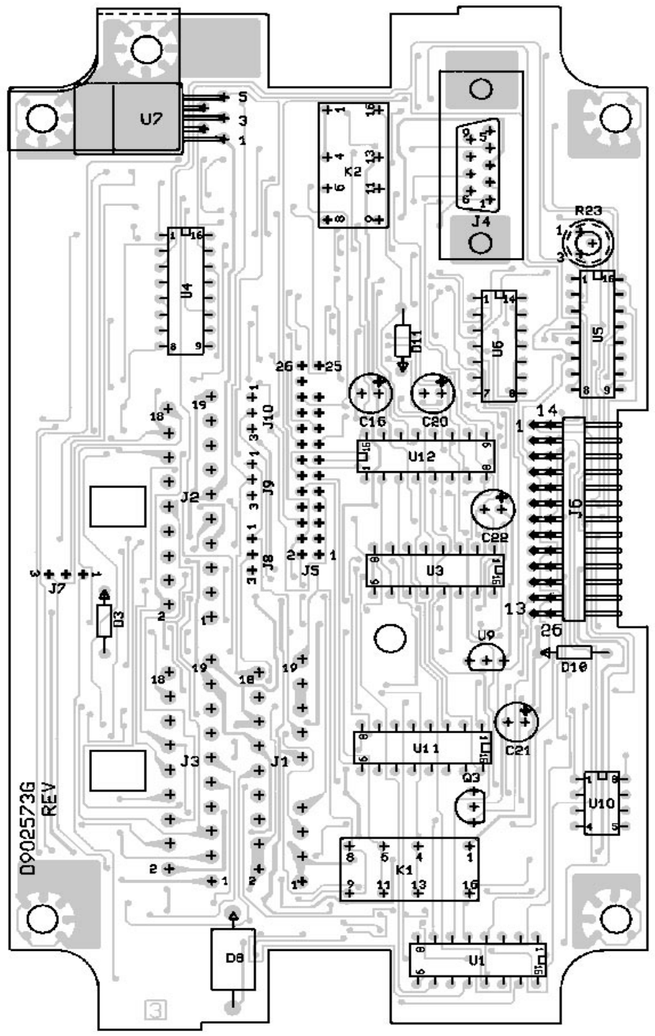
### MULTIPLEXER U1
### 19A700029P36



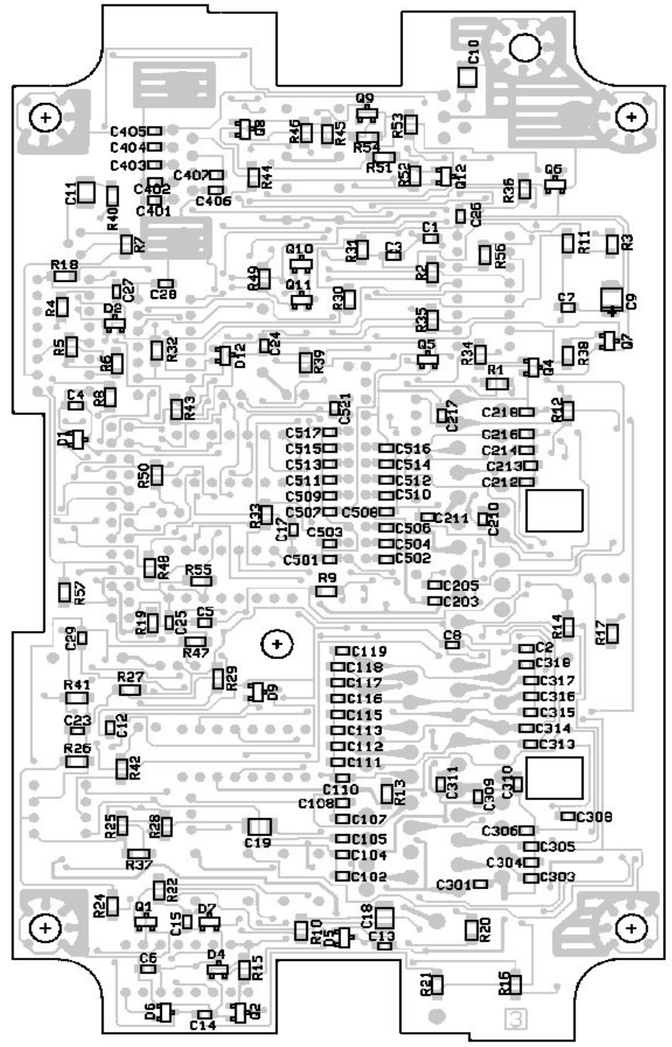

VDD =PIN 16
VSS =PIN8
VEE =PIN 7

COMPONENT SIDE




(19D902573, Rev. 0)
(19D902572, Component Side, Rev. 3)

SOLDER SIDE




(19D902573, Rev. 0)
(19D902572, Solder Side, Rev. 3)

CHIP TRANSISTOR IDENTIFICATION


CHIP DIODE IDENTIFICATION


LEAD IDENTIFICATION
U9


IN-LINE
TOP VIEW
NOTE:CASE SHAPE IS DETERMINING FACTOR FOR LEAD IDENTIFICATION

LEAD IDENTIFICATION
Q3


IN-LINE
TOP VIEW
NOTE:CASE SHAPE IS DETERMINING FACTOR FOR LEAD IDENTIFICATION

JUMPER CHART

| JUMPER | POSITION | DESCRIPTION |
|---|---|---|
| P7 | 1 & 2 | GROUP DOWN OPTION |
| | 2 & 3 | DEFAULT |
| P8 | 1 & 2 | DEFAULT |
| | 2 & 3 | HANDSET/HOOKSWITCH OPTION |
| P9 | 1 & 2 | DEFAULT |
| | 2 & 3 | HANDSET/HOOKSWITCH OPTION |
| P10 | 1 & 2 | EXTERNAL SPEAKER DISABLE |
| | 2 & 3 | DEFAULT |

CAUTION
OBSERVE PRECAUTIONS FOR HANDLING ELECTROSTATIC SENSITIVE DEVICES

**I/O BOARD**

**INPUT/OUTPUT BOARD**
**19D902573G1**
**ISSUE 2**

| SYMBOL | PART NO. | DESCRIPTION |
|---|---|---|
| | | - - - - - - - - - - CAPACITORS - - - - - - - - - |
| C1 and C2 | 19A702236P50 | Ceramic: 100 pF ±5%, 50 VDCW, temp coef 0±30 PPM/°C. |
| C3 thru C7 | 19A702052P5 | Ceramic: 1000 pF ±10%, 50 VDCW. |
| C8 | 19A702236P50 | Ceramic: 100 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C. |
| C9 | 19A705205P3 | Tantalum: 2.2 µF, 10 VDCW; sim to Sprague 293D. |
| C10 and C11 | 19A702052P26 | Ceramic: 0.1 µF ± 10%, 50 VDCW. |
| C12 thru C15 | 19A702052P5 | Ceramic: 1000 pF ±10%, 50 VDCW. |
| C16 | 19A704879P2 | Electrolytic: 47 µF ±20%, 16 VDCW. |
| C17 | 19A702052P3 | Ceramic: 470 pF ± 10%, 50 VDCW. |
| C18 and C19 | 19A702052P26 | Ceramic: 0.1 µF ± 10%, 50 VDCW. |
| C20 thru C22 | 19A704879P2 | Electrolytic: 47 µF ±20%, 16 VDCW. |
| C23 and C24 | 19A702052P5 | Ceramic: 1000 pF ±10%, 50 VDCW. |
| C25 thru C29 | 19A702052P14 | Ceramic: 0.01 µF ± 10%, 50 VDCW. |
| C102 | 19A702052P3 | Ceramic: 470 pF ± 10%, 50 VDCW. |
| C104 and C105 | 19A702052P3 | Ceramic: 470 pF ± 10%, 50 VDCW. |
| C107 and C108 | 19A702052P3 | Ceramic: 470 pF ± 10%, 50 VDCW. |
| C110 thru C113 | 19A702052P3 | Ceramic: 470 pF ± 10%, 50 VDCW. |
| C115 thru C119 | 19A702052P3 | Ceramic: 470 pF ± 10%, 50 VDCW. |
| C203 | 19A702052P3 | Ceramic: 470 pF ± 10%, 50 VDCW. |
| C205 | 19A702052P3 | Ceramic: 470 pF ± 10%, 50 VDCW. |
| C210 thru C214 | 19A702052P3 | Ceramic: 470 pF ± 10%, 50 VDCW. |
| C216 thru C218 | 19A702052P3 | Ceramic: 470 pF ± 10%, 50 VDCW. |
| C301 | 19A702052P3 | Ceramic: 470 pF ± 10%, 50 VDCW. |
| C303 thru C306 | 19A702052P3 | Ceramic: 470 pF ± 10%, 50 VDCW. |
| C308 thru C311 | 19A702052P3 | Ceramic: 470 pF ± 10%, 50 VDCW. |
| C313 thru C318 | 19A702052P3 | Ceramic: 470 pF ± 10%, 50 VDCW. |
| C401 thru C407 | 19A702052P3 | Ceramic: 470 pF ± 10%, 50 VDCW. |
| C501 thru C504 | 19A702052P3 | Ceramic: 470 pF ± 10%, 50 VDCW. |
| C506 thru C517 | 19A702052P3 | Ceramic: 470 pF ± 10%, 50 VDCW. |
| C521 | 19A702052P3 | Ceramic: 470 pF ± 10%, 50 VDCW. |
| | | - - - - - - - - - - DIODES - - - - - - - - - - |
| D1 and D2 | 19A700053P2 | Silicon: 2 Diodes in Series; sim to BAV99. |
| D3 | T324ADP1041 | Silicon: Rectifier; sim to 1N4004. |
| D4 thru D7 | 19A700053P2 | Silicon: 2 Diodes in Series; sim to BAV99. |
| D8 | 19A703588P3 | Zener, transient suppressor: sim to 1N6278A. |
| D9 | 19A700053P2 | Silicon: 2 Diodes in Series; sim to BAV99. |
| D10 and D11 | T324ADP1041 | Silicon: Rectifier; sim to 1N4004. |
| D12 | 19A700053P2 | Silicon: 2 Diodes in Series; sim to BAV99. |
| | | - - - - - - - - - - JACKS - - - - - - - - - - |
| J1 thru J3 | 19A701785P2 | Contact, electrical; sim to Molex -08-50-0404. |
| J4 | 19B209727P35 | Connector, plug. |
| J5 | 19A703248P11 | Post: Gold Plated, 10 mm length. |
| J6 | 19A702333P55 | Connector, header; sim to Dupont 79257-126. |
| J7 thru J10 | 19A703248P11 | Post: Gold Plated, 10 mm length. |
| K1 and K2 | 19B235003P1 | Relay: sim to AROMAT DS2E-N-12V. |
| | | - - - - - - - - - - PLUGS - - - - - - - - - - |
| P7 thru P10 | 19A702104P3 | Connector: two position shorting; sim to Du-pont 68786-202. |
| | | - - - - - - - - - - TRANSISTORS - - - - - - - - - |
| Q1 and Q2 | 19A700076P2 | Silicon, NPN: sim to MMBT3904, low profile. |
| Q3 | 19A702503P2 | Silicon, NPN: sim to 2N4401. |
| Q4 thru Q7 | 19A700076P2 | Silicon, NPN: sim to MMBT3904, low profile. |
| Q8 and Q9 | 19A700059P2 | Silicon, PNP: sim to MMBT3906, low profile. |
| Q10 thru Q12 | 19A700076P2 | Silicon, NPN: sim to MMBT3904, low profile. |
| | | - - - - - - - - - - RESISTORS - - - - - - - - - - |
| R1 | 19B800607P101 | Metal film: 100 ohms ±5%, 1/8 w. |
| R2 | 19B800607P470 | Metal film: 47 ohms ±5%, 1/8 w. |
| R3 | 19B800607P101 | Metal film: 100 ohms ±5%, 1/8 w. |
| R4 | 19A702931P458 | Metal film: 382K ohms ±1%, 200 VDCW, 1/8 w. |
| R5 | 19A702931P430 | Metal film: 200K ohms ±1%, 200 VDCW, 1/8 w. |
| R6 | 19A702931P401 | Metal film: 100K ohms ±1%, 200 VDCW, 1/8 w. |
| R7 | 19A702931P368 | Metal film: 49.9K ohms ±1%, 200 VDCW, 1/8 w. |
| R8 | 19A702931P339 | Metal film: 24.9K ohms ±1%, 200 VDCW, 1/8 w. |
| R9 thru R11 | 19B800607P101 | Metal film: 100 ohms ±5%, 1/8 w. |
| R12 | 19B800607P470 | Metal film: 47 ohms ±5%, 1/8 w. |
| R13 and R14 | 19B800607P104 | Metal film: 100K ohms ±5%, 1/8 w. |
| R15 thru R18 | 19B800607P103 | Metal film: 10K ohms ±5%, 1/8 w. |
| R19 | 19B800607P272 | Metal film: 2.7K ohms ±5%, 1/8 w. |
| R20 thru R22 | 19B800607P101 | Metal film: 100 ohms ±5%, 1/8 w. |
| R23 | 19A700016P4 | Variable, cermet: 10K ohms ±10%, 1/2 w; sim to Bourns 3329H-1-103. |
| R24 and R25 | 19B800607P104 | Metal film: 100K ohms ±5%, 1/8 w. |
| R26 | 19A702931P349 | Metal film: 31.6K ohms ±1%, 200 VDCW, 1/8 w. |
| R27 | 19B800607P102 | Metal film: 1K ohms ±5%, 1/8 w. |
| R28 and R29 | 19B800607P223 | Metal film: 22K ohms ±5%, 1/8 w. |
| R30 and R31 | 19B800607P104 | Metal film: 100K ohms ±5%, 1/8 w. |
| R32 | 19B800607P103 | Metal film: 10K ohms ±5%, 1/8 w. |
| R33 | 19B800607P101 | Metal film: 100 ohms ±5%, 1/8 w. |
| R34 thru R36 | 19B800607P223 | Metal film: 22K ohms ±5%, 1/8 w. |
| R37 | 19A702931P349 | Metal film: 31.6K ohms ±1%, 200 VDCW, 1/8 w. |
| R38 | 19B800607P223 | Metal film: 22K ohms ±5%, 1/8 w. |
| R39 | 19B800607P101 | Metal film: 100 ohms ±5%, 1/8 w. |
| R40 and R41 | 19B800607P223 | Metal film: 22K ohms ±5%, 1/8 w. |
| R42 | 19B800607P104 | Metal film: 100K ohms ±5%, 1/8 w. |
| R43 | 19B800607P102 | Metal film: 1K ohms ±5%, 1/8 w. |
| R44 | 19B800607P471 | Metal film: 470 ohms ±5%, 1/8 w. |
| R45 | 19B800607P104 | Metal film: 100K ohms ±5%, 1/8 w. |
| R46 thru R53 | 19B800607P223 | Metal film: 22K ohms ±5%, 1/8 w. |
| R54 thru R57 | 19B800607P104 | Metal film: 100K ohms ±5%, 1/8 w. |
| | | - - - - - - - - INTEGRATED CIRCUITS - - - - - - - |
| U1 | 19A700029P36 | Digital: Single 8-Channel Multiplexer; sim to 4051B. |
| U3 and U4 | 19A703471P9 | Digital: 8 Bit Latch / 1 of 8 Decoder; sim to 74HC259. |
| U5 | 19A704380P9 | Digital: CMOS Hex Data Flip-Flop; sim to 74HC174. |
| U6 | 19A116180P75 | Digital: Hex Open Collector Inverter; sim to 7406. |
| U7 | 19A704970P1 | Linear: 5 Volt Regulator with Reset Output; sim to SGS L387. |
| U9 | 19A704971P1 | Linear: +5 Volt Regulator; sim to MC78L05ACP. |
| U10 | 19A701789P2 | Linear: Dual Op Amp; sim to LM358. |
| U11 and U12 | 19A134693P1 | Interface: 7 Darlington Transistor Arrays; sim to ULN-2003A. |
| | | - - - - - - - - - - MISCELLANEOUS - - - - - - - - - |
| 4 | N404P11B6 | Lockwasher, internal tooth, No. 4. |
| 8 | N80P9006B6 | Screw, Machine: Pan Head; 4-40 x 3/8". |
| 9 | 7141225P2 | Nut, Hex: 4-40. |
| 10 | 19B234894P1 | Plate. |
| 11 | 19A143578P67 | Spacer, threaded, metallic. |

*COMPONENTS ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES

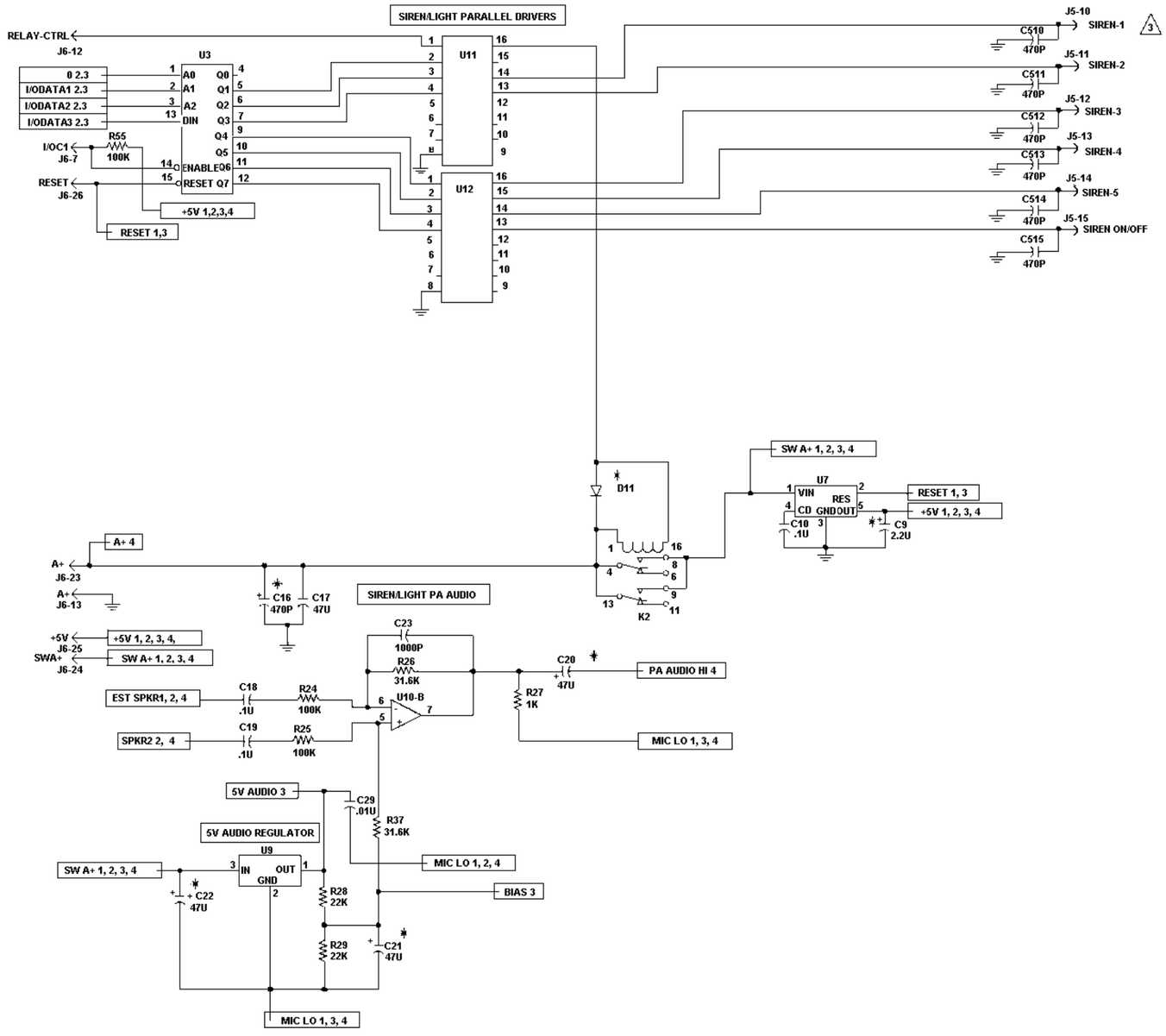



TABLE 1
POWER AND GROUND CONNECTIONS CHART

| DEVICE | +5V | GND | 5V AUDIO | MIC LO | A+SW |
|---|---|---|---|---|---|
| U1 | 16 | 7,8 | | | |
| U3, C25 | 16 | 8 | | | |
| U4, C26 | 16 | 8 | | | |
| U5, C27 | 16 | 8 | | | |
| U6, C28 | 14 | 7 | | | |
| U7 | 5 | 3 | | | 1 |
| U8 | | | 1 | 2 | 3 |
| U10, C29 | | | 8 | 4 | |
| U11 | | 8 | | | |
| U12 | | 8 | | | |

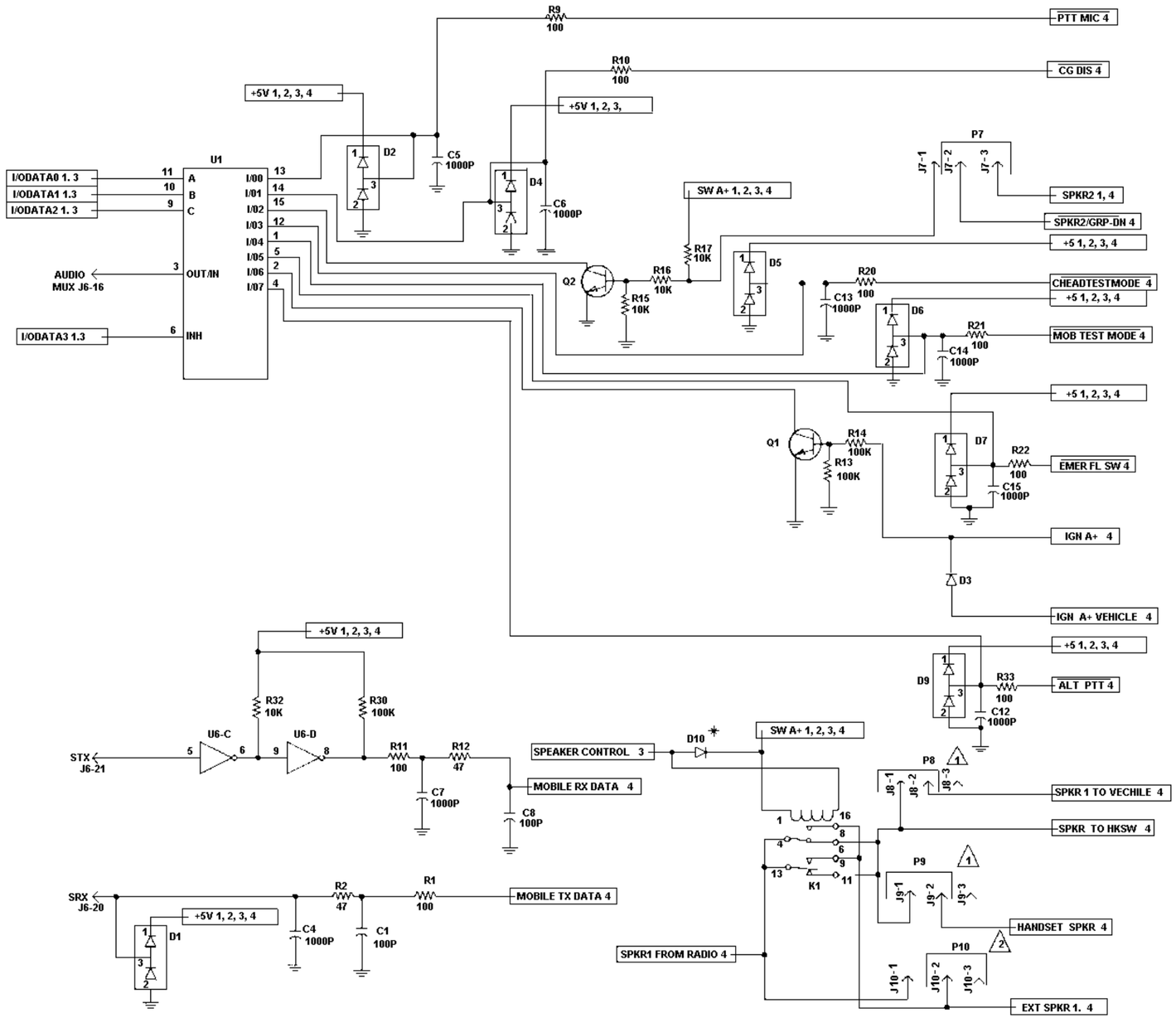
ALL DIODES, CAPACITORS, RESISTORS, AND TRANSISTORS ARE CHIP COMPONENTS ON THE SOLDER SIDE OF THE BOARD UNLESS FOLLOWED BY ✶

| THIS SCHEMATIC DIAG. APPLIES TO | |
|---|---|
| MODEL NO. | REV LETTER |
| | |

ALL RESISTORS ARE 0.1 WATT UNLESS OTHERWISE SPECIFIED AND RESISTOR VALUES IN OHMS UNLESS FOLLOWED BY MULTIPLIER K OR M.
CAPACITOR VALUES IN F UNLESS FOLLOWED BY MULTIPLIER U, N OR P
INDUCTANCE VALUES IN H UNLESS FOLLOWED BY MULTIPLIER M OR U.

**I/O BOARD**
**SHEET 1**

(19D902575, Sh. 1, Rev. 0)



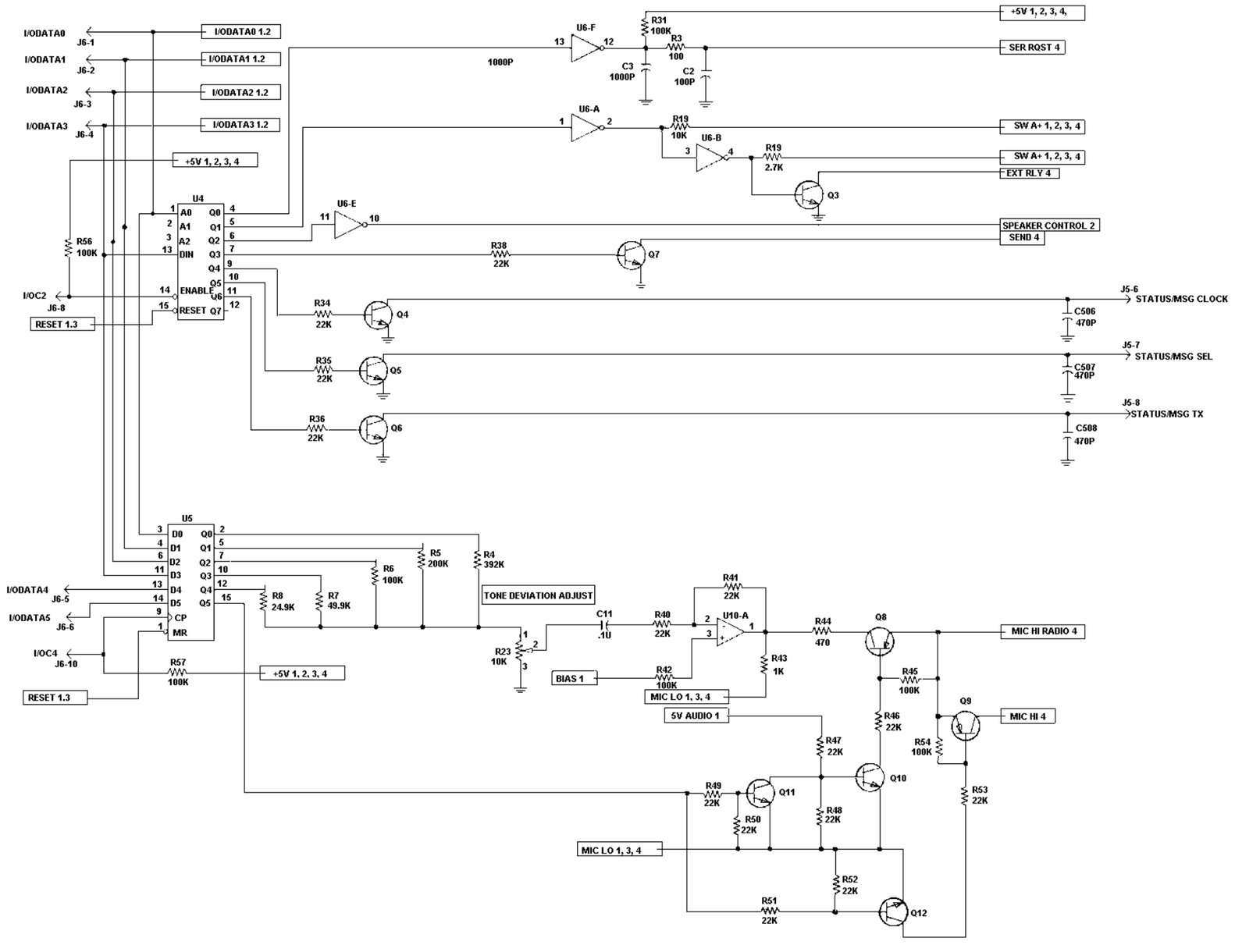

| PLUG | CONNECTION | DESCRIPTION |
|---|---|---|
| P7 | J7-1&2 | OPTION |
| P7 | J7-2&3 | STANDARD SPKR 2 |
| P8 | J8-1&2 | "C" JUMPER STANDARD |
| P8 | J8-2&3 | HANDSET/HOOKSWITCH OPTION |
| P9 | J9-1&2 | "A" JUMPER STANDARD |
| P9 | J9-2&3 | HANSET/HOOKSWITCH OPTION |
| P10 | J10-1&2 | DUAL CONTROL WITH PARALLEL AUDIO OPTION |
| P10 | J10-2&3 | "N" JUMPER STANDARD |

NOTES:

1. FOR HANDSSET/HOOKSWITCH MOVE P8 TO J8-2&3 AND MOVE P9 TO J9-2&3
2. FOR DUAL COVER CONTROL WI TH PARALLEL AUDIO MOVE P10 TO J10-1&2
3. RELAYS CONNECTED DIRECTLY TO THE PARALLEL SIREN OUTPUTS MUST HAVE REVERSE EMF PROTECTION DIDOES INSTALLED ON THE RELAYS.

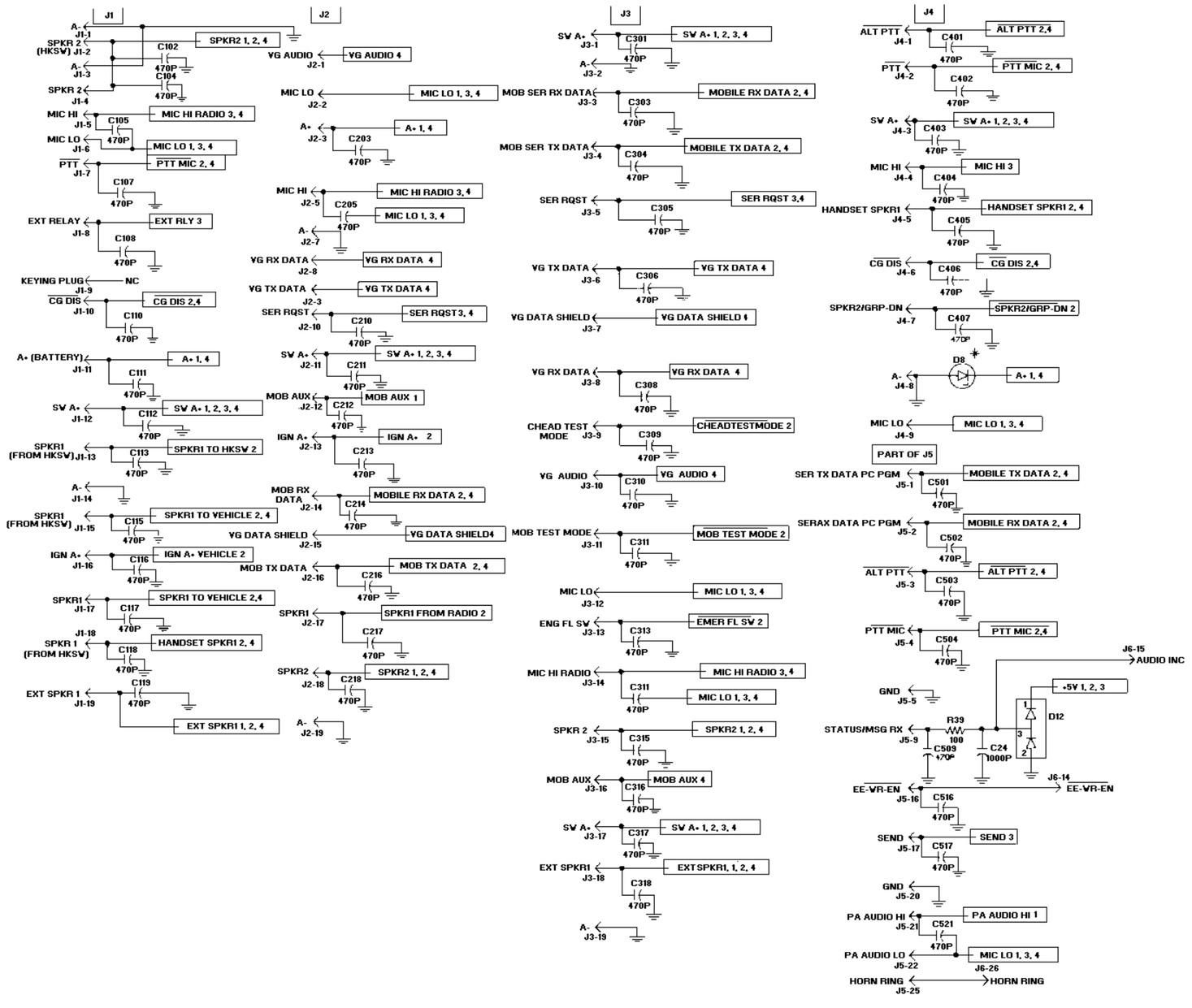
## I/O BOARD SHEET 2

(19D902575, Sh. 2, Rev. 0)




**I/O BOARD**
**SHEET 3**

(19D902575, Sh. 3, Rev. 0)




## I/O BOARD SHEET 4

(19D902575, Sh. 4, Rev. 0)

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